TI TPS659037 PMIC - BOTTOM VIEW (balls facing you)

169-ball ZWS nFBGA, 12 x 12 mm, 0.8 mm pitch. PMIC on the CompuLab CL-SOM-AM57x.
Source: TI datasheet SLIS165G, Figure 3-1 (top view), mirrored left-right here.

	N	M	L	K	J	H	G	F	E	D	C	B	A
13	N13 PBKG	M13 GND_ANA	L13 LDO34_IN	K13 SMPS3 FDBK	J13 SMPS3_SW	H13 SMPS3_IN	G13 SMPS2_IN	F13 SMPS2_SW	E13 SMPS1_SW	D13 SMPS1_IN	C13 GPIO_1	B13 SMPS1_2 FDBK	A13 PBKG
12	N12 VPROG	M12 GND_DIG	L12 LDO34_IN	K12 LDO4_OUT	J12 SMPS3_SW	H12 SMPS3_IN	G12 SMPS2_IN	F12 SMPS2_SW	E12 SMPS1_SW	D12 SMPS1_IN	C12 SMPS1_2 FDBK_GND	B12 GPIO_0	A12 GPIO_2
11	N11 GPIO_6	M11 CLK32KGO	L11 SMPS8 FDBK	K11 LDO3_OUT	J11 SMPS3_SW	H11 SMPS3_IN	G11 SMPS2_IN	F11 SMPS2_SW	E11 SMPS1_SW	D11 SMPS1_IN	C11 RPWRON	B11 PBKG	A11 VCC SENSE2
10	N10 SMPS8_SW	M10 SMPS8_SW	L10 SMPS8 GND	K10 GPIO_4	J10 SMPS3 GND	H10 SMPS3 GND	G10 SMPS2 GND	F10 SMPS2 GND	E10 SMPS1 GND	D10 SMPS1 GND	C10 GPIO_5	B10 PBKG	A10 LDOUSB IN1
9	N9 SMPS8_IN	M9 SMPS8_IN	L9 SMPS8 GND	K9 RESET_IN	J9 SMPS3 GND	H9 GPIO_3	G9 GPIO_7	F9 SMPS2 GND	E9 SMPS1 GND	D9 VIO_IN	C9 NC	B9 LDOUSB OUT	A9 LDOUSB IN2
8	N8 SMPS9_IN	M8 SMPS9_IN	L8 SMPS9 GND	K8 PWRDOWN	J8 SMPS9 FDBK	H8 I2C2_SDA SDO	G8 PWRON	F8 REGEN1	E8 PBKG	D8 VBUS	C8 LDOVANA OUT	B8 SYNCDCDC	A8 LDOVRTC OUT
7	N7 SMPS9_SW	M7 SMPS9_SW	L7 SMPS9 GND	K7 BOOT1	J7 POWERGOOD	H7 PBKG	G7 PBKG	F7 PBKG	E7 GND_ANA	D7 PBKG	C7 VCC1	B7 VBG	A7 GND_ANA
6	N6 SMPS6_IN	M6 SMPS6_IN	L6 SMPS6 GND	K6 SMPS6 FDBK	J6 PBKG	H6 PBKG	G6 RESET_OUT	F6 PBKG	E6 NRESWARM	D6 PBKG	C6 LDO1_OUT	B6 LDO2_OUT	A6 LDO12_IN
5	N5 SMPS6_SW	M5 SMPS6_SW	L5 SMPS6 GND	K5 NC	J5 ENABLE1	H5 SMPS5 GND	G5 SMPS4 GND	F5 GND_ANA	E5 NSLEEP	D5 SMPS7 GND	C5 LDOLN_IN	B5 LDOLN_OUT	A5 LDO9_OUT
4	N4 LDO SUPPLY	M4 LDO SUPPLY	L4 NC	K4 NC	J4 SMPS5 GND	H4 SMPS5 GND	G4 SMPS4 GND	F4 SMPS4 GND	E4 SMPS7 GND	D4 SMPS7 GND	C4 LDO9_IN	B4 GPADC VREF	A4 REFGND1
3	N3 LDO SUPPLY	M3 I2C2_SCL SCE	L3 BOOT0	K3 SMPS4_5 FDBK_GND	J3 SMPS5_IN	H3 SMPS5_SW	G3 SMPS4_SW	F3 SMPS4_IN	E3 SMPS7_IN	D3 SMPS7_SW	C3 GPADC_IN2	B3 VCC_SENSE	A3 OSC16MIN
2	N2 VIO_GND	M2 PBKG	L2 I2C1_SDA SDI	K2 SMPS4_5 FDBK	J2 SMPS5_IN	H2 SMPS5_SW	G2 SMPS4_SW	F2 SMPS4_IN	E2 SMPS7_IN	D2 SMPS7_SW	C2 GPADC_IN1	B2 GPADC_IN0	A2 OSC16MOUT
1	N1 PBKG	M1 PBKG	L1 I2C1_SCL SCK	K1 INT	J1 SMPS5_IN	H1 SMPS5_SW	G1 SMPS4_SW	F1 SMPS4_IN	E1 SMPS7_IN	D1 SMPS7_SW	C1 OSC16MCAP	B1 SMPS7 FDBK	A1 PBKG

A1 corner (bottom right in this view)

- SMPS1..9_IN, VCC1, LDO_SUPPLY: power inputs from the system supply (VSYS, 5 V on this module)
- VCC_SENSE, VCC_SENSE2: system-supply sense lines (also on VSYS, low current)
- LDO inputs and VIO_IN: datasheet says "system supply", but designs often feed these from another rail
- Ground: PBKG (substrate), SMPSx_GND (power), GND_ANA, GND_DIG, REFGND1, VIO_GND
- SMPS1_2_FDBK_GND, SMPS4_5_FDBK_GND: ground-sense feedback inputs
- SMPSx_SW: switch nodes, go to the inductors. A failed high-side switch shorts SMPSx_IN to SMPSx_SW
- Other signals

Which of the orange inputs CompuLab tied to VSYS is not documented. Check on the board (pads or nearby caps) before relying on it.
In the top-view datasheet figure column A is on the left; this page shows the package flipped, as seen when looking at the balls or the PCB land pattern.